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Japanese Patent Laid-Open Publication No. Heisei 9-8205

[TITLE OF THE INVENTION]

RESIN-ENCAPSULATED SEMICONDUCTOR DEVICE

5

[CLAIMS]

1. A resin-encapsulated semiconductor device using
a lead frame which is shaped in accordance with a two-step
etching process to a body wherein a thickness of inner
10 leads is less than that of the lead frame blank,
comprising:

inner leads having the thickness less than that of the
lead frame blank; and

15 terminal columns integrally connected to the inner
leads and having the same thickness with the lead frame
blank, the terminal columns possessing a column-shaped
configuration which is adapted to be electrically connected
to an external circuit, the terminal columns being disposed
20 outside of the inner leads in a manner such that they are
coupled to the inner leads in a direction orthogonal to the
thickness-wise direction thereof, the terminal columns
having terminal portions arranged on top ends thereof, the
terminal portions being made of solders, etc. and exposed
25 to the outside beyond a resin encapsulate, each inner lead
possessing a rectangular cross-section and having four

surfaces including a first surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surface of a remaining portion of the inner lead having the same thickness with the lead frame blank while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the inside of the inner lead.

2. A resin-encapsulated semiconductor device using a lead frame which is shaped in accordance with a two-step etching process to a body wherein a thickness of inner leads is less than that of the lead frame blank, comprising:

inner leads having the thickness less than that of the lead frame blank; and
terminal columns integrally connected to the inner leads and having the same thickness with the lead frame blank, the terminal columns possessing a column-shaped configuration which is adapted to be electrically connected to an external circuit, the terminal columns being disposed outside of the inner leads in a manner such that they are coupled to the inner leads in a direction orthogonal to the thickness-wise direction thereof, portions of top ends of the terminal columns being exposed to the outside beyond a resin encapsulate, each inner lead possessing a rectangular

cross-section and having four surfaces including a first surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surface of a remaining portion of the inner lead having the same thickness with the lead frame blank while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the inside of the inner lead.

10 3. The resin-encapsulated semiconductor device as claimed in claims 1 or 2, wherein a semiconductor chip is received inward of the inner leads, and electrodes of the semiconductor chip are electrically connected to the inner leads through wires, respectively.

15 4. The resin-encapsulated semiconductor device as claimed in claim 3, wherein the lead frame has a die pad, and the semiconductor chip is mounted onto the die pad.

20 5. The resin-encapsulated semiconductor device as claimed in claim 3, wherein the lead frame does not have a die pad, and the semiconductor chip is fastened to the inner leads using a reinforcing fastener tape.

25 6. The resin-encapsulated semiconductor device as

claimed in claims 1 or 2, wherein the semiconductor chip is
fastened by means of insulating adhesive to the second
surfaces of the inner leads on one surface thereof on which
the electrodes are located, and the electrodes of the
5 semiconductor chip are electrically connected to the first
surfaces of the inner leads through wires, respectively.

7. The resin-encapsulated semiconductor device as
claimed in claims 1 or 2, wherein the semiconductor chip is
10 fastened to the second surfaces of the inner leads by bumps
thereby to be electrically connected to the inner leads.

[DETAILED DESCRIPTION OF THE INVENTION]

[FIELD OF THE INVENTION]

15 The present invention relates to a resin-
encapsulated semiconductor device capable of meeting the
requirement for an increase in the number of terminals and
resolving problems which are caused in association with
position shift and coplanarity of an outer lead.

20

[DESCRIPTION OF THE PRIOR ART]

FIG. 15(a) shows the configuration of a generally
known resin-encapsulated semiconductor device (a plastic
lead frame package). The shown resin-encapsulated
25 semiconductor device includes a die pad 1511 having a

semiconductor chip 1520 mounted thereon, outer leads 1513
to be electrically connected to the associated circuits,
inner leads 1512 formed integrally with the outer leads
1513, bonding wires 1530 for electrically connecting the
tips of the inner leads 1512 to the bonding pad 1521 of the
semiconductor chip 1520, and a resin 1540 encapsulating the
semiconductor chip 1520 to protect the semiconductor chip
1520 from external stresses and contaminants. This resin-
encapsulated semiconductor device, after mounting the
semiconductor chip 1520 on the bonding pad 1521, is
manufactured by encapsulating the semiconductor chip 1520
with the resin. In this resin-encapsulated semiconductor
device, the number of the inner leads 1512 is equal to that
of the bonding pads 1521 of the semiconductor chip 1520.
And, FIG. 15(b) shows the configuration of a monolayer lead
frame used as an assembly member of the resin-encapsulated
semiconductor device shown in FIG. 15a. Such a lead frame
includes the bonding pad 1511 for mounting the
semiconductor chip, the inner leads 1512 to be electrically
connected to the semiconductor chip, the outer lead 1513
which is integral with the inner leads 1512 and is to be
electrically connected to the associated circuits. This
also includes dam bars 1514 serving as a dam when
encapsulating the semiconductor chip with the resin, and a
frame 1515 serving to support the entire lead frame 1510.

Such a lead frame is formed from a highly conductive metal such as a cobalt, 42 alloy (a 42% Ni-Fe alloy), copper-cased alloy by a pressing working process or an etching process. FIG. 15(b)(D) is a cross-sectional view taken along the line F1-F2 of FIG. 15(b)(1).

Recently, there has been growing demand for the miniaturization and reduction in thickness of resin-encapsulated semiconductor device employing lead frames like the lead frame (plastic lead frame package) and the increase of the number of terminals of resin-encapsulated semiconductor package as electronic apparatuses are miniaturized progressively and the degree of the integration of semiconductor device increase progressively. Thus, recent resin-encapsulated semiconductor package, particularly quad plate package (QFPs) and thin quad flat packages (TQFPs) have each a greatly increased number of pins.

Lead frames having inner leads arranged at small pitches among lead frames for semiconductor packages are fabricated by a photolithographic etching process, while lead frames having inner leads arranged at comparatively large pitches among lead frames for semiconductor packages are fabricated by press working. However, lead frames having a large number of fine inner leads to be used for forming semiconductor packages having a large number of

pins are fabricated by subjecting a blank of a thickness on the order of 0.25 mm to an etching process, not a press working.

5 The etching process for forming a lead frame having fine inner leads will be described hereinafter with reference to FIG. 14. First, a copper alloy or 42 alloy thin sheet of a thickness on the order of 0.25 mm (a lead frame blank 1410) is cleaned perfectly (FIG. 14(a)). Then, a photoresist, such as a water-soluble casein photoresist containing potassium dichromate as a sensitive agent, is spread in photoresist films 1420 over the major surfaces of the thin film as shown in FIG. 14(b).

10 Then, the photoresist films are exposed, through a mask of a predetermined pattern, to light emitted by a high-pressure mercury lamp, and the thin sheet is immersed in a developer for development to form a patterned photoresist film 1430 as shown in FIG. 14(c). Then, the thin sheet is subjected, when need be, to a hardening process, a washing process and such, and then an etchant containing ferric chloride as a principal component is sprayed against the thin sheet 1410 to etch through portions of the thin sheet 1410 not coated with the patterned photoresist films 1020 so that inner leads of predetermined sizes and shapes are formed as shown in FIG. 14(d).

Then, the patterned resist films are removed, the patterned thin sheet 1410 is washed to complete a lead frame having the inner leads of desired shapes as shown in FIG. 14(e). Predetermined areas of the lead frame thus
5 formed by the etching process are silver-plated. After being washed and dried, an adhesive polyimide tape is stuck to the inner leads for fixation, predetermined tab bars are bent, when need be, and the die pad depressed. In the etching process, the etchant etches the thin sheet in both
10 the direction of the thickness and directions perpendicular to the thickness, which limits the miniaturization of inner lead pitches of lead frames. Since the thin sheet is etched from both the major surfaces as shown in FIG. 14 during the etching process, it is said, when the lead frame
15 has a line-and-space shape, that the smallest possible intervals between the lines are in the range of 50 to 100% of the thickness of the thin sheet. From the viewpoint of forming the outer lead having a sufficient strength, generally, the thickness of the thin sheet must be about
20 0.125 mm or above. Furthermore, the width of the inner leads must be in the range of 70 to 80 μ m for successful wire bonding. When the etching process as illustrated in FIG. 14 is employed in fabricating a lead frame, a thin sheet of a small thickness in the range of 0.125 to 0.15 mm
25 is used and inner leads are formed by etching so that th

fine tips thereof are arranged at a pitch of about 0.1 mm.

However, recent miniature resin-encapsulated semiconductor package requires inner leads arranged
5 pitches in the range of 0.13 to 0.15 mm, far smaller than 0.165 mm. When a lead frame is fabricated by processing thin sheet of a reduced thickness, the strength of the outer leads of such a lead frame is not large enough
10 withstand external forces that may be applied thereto in the subsequent processes including an assembling process and a chip mounting process. Accordingly, there is a limit to the reduction of the thickness of the thin sheet to enable the fabrication of a minute lead frame having fine leads arranged at very small pitches by etching.

15 An etching method previously proposed to overcome such difficulties subjects a thin sheet to an etching process to form a lead frame after reducing the thickness of portions of the thin sheet corresponding to the inner leads of the lead frame by half etching or pressing to form
20 the fine inner leads by etching without reducing the strength of the outer leads. However, problems arise in accuracy in the subsequent processes when the lead frame is formed by etching after reducing the thickness of the portions corresponding to the inner leads by pressing; for
25 example, the smoothness of the surface of the plated areas

is unsatisfactory, the inner leads cannot be formed in a flatness and a dimensional accuracy required to clamp the lead frame accurately for bonding and molding, and a platemaking process must be repeated twice making the lead fabricating process intricate. It is also necessary to repeat a platemaking process twice when the thickness of the portions of the thin sheet corresponding to the inner leads is reduced by half etching before subjecting the thin sheet to an etching process for forming the lead frame, which also makes the lead frame fabricating process intricate. Thus, this previously proposed etching method has not yet been applied to practical lead frame fabricating processes.

(SUBJECT MATTERS TO BE SOLVED BY THE INVENTION)

On the other hand, because a pitch among inner leads is made narrow as the number of terminals is increased, it is considered important to know whether a problem is caused or not in association with position shift or coplanarity of an outer lead when implementing a chip mounting process. Accordingly, the present invention has been made in an effort to solve the problems occurring in the related art, and an object of the present invention is to provide a resin-encapsulated semiconductor device capable of meeting the requirement for an increase in the number of terminals

and resolving problems which are caused in association with position shift and coplanarity of an outer lead.

[MEANS FOR SOLVING THE SUBJECT MATTERS:]

5 According to one aspect of the present invention there is provided a resin-encapsulated semiconductor device using a lead frame which is shaped in accordance with a two-step etching process to a body wherein a thickness of inner leads is less than that of the lead frame blank comprising: inner leads having the thickness less than
10 of the lead frame blank; and terminal columns electrically connected to the inner leads and having the same thickness as with the lead frame blank, the terminal columns possessing a column-shaped configuration which is adapted to be
15 electrically connected to an external circuit, the terminal columns being disposed outside of the inner leads in a manner such that they are coupled to the inner leads in a direction orthogonal to the thickness-wise direction thereof, the terminal columns having terminal portions
20 arranged on top ends thereof, the terminal portions being made of solders, etc. and exposed to the outside beyond the resin encapsulate, outer surfaces of the terminal columns also being exposed to the outside beyond the resin encapsulate, each inner lead possessing a rectangular
25 cross-section and having four surfaces including a

surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surf of a remaining portion of the inner lead having the same thickness with the lead frame blank while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the inside of the inner lead.

According to another aspect of the present invention there is provided a resin-encapsulated semiconductor device using a lead frame which is shaped in accordance with a two-step etching process to a body wherein a thickness of inner leads is less than that of the lead frame blank comprising: inner leads having the thickness less than that of the lead frame blank; and terminal columns integrally connected to the inner leads and having the same thickness with the lead frame blank, the terminal columns possessing a column-shaped configuration which is adapted to be electrically connected to an external circuit, the terminal columns being disposed outside of the inner leads in a manner such that they are coupled to the inner leads in a direction orthogonal to the thickness-wise direction thereof, portions of top ends of the terminal columns being exposed to the outside beyond a resin encapsulate, outer surfaces of the terminal columns also being exposed to the outside beyond the resin encapsulate, each inner lead

possessing a rectangular cross-section and having four surfaces including a first surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surface of a remaining portion of the inner lead having the same thickness with the lead frame blank while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the inside of the inner lead.

According to another aspect of the present invention, a semiconductor chip is received inward of the inner leads, and electrodes (pads) of the semiconductor chip are electrically connected to the inner leads through wires, respectively. According to another aspect of the present invention, the lead frame has a die pad, and the semiconductor chip is mounted onto the die pad. According to another aspect of the present invention, the lead frame does not have a die pad, and the semiconductor chip is fastened to the inner leads using a reinforcing fastener tape. According to still another aspect of the present invention, the semiconductor chip is fastened by means of insulating adhesive to the second surfaces of the inner leads on one surface thereof on which the electrodes are located, and the electrodes of the semiconductor chip are electrically connected to the first surfaces of the inner leads through wires, respectively. According to yet still

another aspect of the present invention, the semiconductor chip is fastened to the second surfaces of the inner leads by bumps thereby to be electrically connected to the inner leads. In the above descriptions, in the case that the terminal columns have terminal portions which are arranged on top ends of the terminal columns, with the terminal portions made of solders, etc. and exposed to the outside beyond the resin encapsulate, while it is the norm that the terminal portions comprising the solders, etc. are exposed to the outside beyond the resin encapsulate, it is not necessarily required for the terminal portions to be projected beyond the resin encapsulate. Moreover, while it is possible to use the outside surfaces of the terminal columns while they are not encapsulated by the resin encapsulate and they are exposed to the outside, the outside surfaces of the terminal columns which are not encapsulated by the resin encapsulate, can be covered by a protective frame using adhesive, etc.

20 (WORKING FUNCTIONS)

The resin-encapsulated semiconductor device in accordance with the present invention can meet a demand for an increase in the number of terminals. At the same time, in the resin-encapsulated semiconductor device, because the forming process of the outer leads as in the case of using

a mono-layered lead frame shown in FIG. 13(b) is not required, it is possible to provide a semiconductor device in which no problems are caused in association with position shift and coplanarity of the outer leads. More particularly, the use of a multi-pinned lead frame shaped in a manner that inner leads have a thickness less than that of the lead frame blank by a two-step etching process, that is, the inner leads are arranged at a fine pitch, can meet a demand for an increase in the pin number of the semiconductor device. Furthermore, by using the lead frame which is fabricated by a two-step etching process as will be described later with reference to FIG. 1, the second surface of each inner lead has coplanarity, and is excellent in wire-bonding property. In addition, since the first surface of the inner lead is also a flat surface and the third and fourth surfaces are depressed toward the inside of the inner lead, the inner leads are stable and coplanarity width upon wire bonding process can be enlarged.

[EMBODIMENTS]

Embodiments of the resin-encapsulated semiconductor device in accordance with the present invention will now be described with reference to the attached drawings. First, a resin-encapsulated semiconductor device in accordance

With a first embodiment of the present invention described hereinafter with reference to FIGS. 1. FIG. 1(a) is a cross-sectional view of the encapsulated semiconductor device according to the embodiment of the present invention. FIG. 1(b) is a sectional view of an inner lead taken along the line of FIG. 1(a), and FIG. 1(c) is a cross-sectional view of a terminal column taken along the line B1-B2 of FIG. 1. Moreover, FIG. 2(a) is a perspective view of the encapsulated semiconductor device according to the embodiment of the present invention, FIG. 2(b) is a view of the resin-encapsulated semiconductor device of FIG. 2(a), and FIG. 2(c) is a bottom view of the encapsulated semiconductor device of FIG. 2(a). In FIGS. 1 and 2, a drawing reference numeral 100 represents an encapsulated semiconductor device, 110 a semiconductor chip, 111 electrodes (pads), 120 wires, 130 a lead, 131 inner leads, 131Aa a first surface, 131Ab a second surface, 131Ac a third surface, 131Ad a fourth surface, 133A terminal columns, 133B terminal portions, 133C top surfaces, 133D a top surface, 135 a die pad, and 140 a resin encapsulate.

In the resin-encapsulated semiconductor device according to the first embodiment, as shown in FIG. 1, the semiconductor chip 110 is placed inward of the

leads 131. As can be readily seen from FIG. 1(a), the semiconductor chip 110 is mounted on the die pad 135 at one surface thereof which is opposed to the other surface thereof where the electrodes (pads) 111 of the semiconductor chip 110 are arranged. Each electrode pad 111 is electrically connected to the second surface 131A of the inner lead 131 through the wire 120. The electrical connection between the resin-encapsulated semiconductor device 100 of this embodiment and an external circuit is achieved by mounting the resin-encapsulated semiconductor device 100 via the terminal portions 133A each being made of a semi-spherical solder, on a printed circuit substrate, with the terminal portions 133A located on the top surfaces 133S of the terminal columns 133, respectively. In the resin-encapsulated semiconductor device of the first embodiment of the present invention, it is not necessarily required to provide a protective frame 190, and instead, a structure, as shown in FIG. 1(d), in which no protective frame is used can be adopted.

The lead frame 130 used in the semiconductor device 100 according to the first embodiment is made of a 42% nickel-iron alloy. Therefore, the lead frame 130A which has a contour as shown in FIG. 9(a) and is shaped by an etching process, is used as the lead frame 130. The lead frame 130 has inner leads 131 which are shaped to have a

thickness less than that of the terminal columns 133 or other portions. Dam bars 136 serve as a dam when encapsulating the semiconductor chip 110 with a resin. Moreover, although the lead frame 130A which is processed by etching to have the contour as shown in FIG. 9A is used in this embodiment, the lead frame is not limited to such a contour because portions except the inner leads 131 and the terminal columns 133 are not necessary. The inner leads 131 have a thickness of 40 μ m whereas the portions of the lead frame 130 other than the inner leads 131 have a thickness of 0.15 mm which corresponds to the thickness of the lead frame blank. The other portions of the lead frame 130 except the inner leads 131 may not have the thickness of 0.15 mm, but have a thickness of 0.125 mm-0.50 mm which is thinner. The tips of the inner leads 131 have a small pitch of 0.12 mm so as to achieve an increase in the number of terminals for semiconductor devices. The second face 131Ab of the inner lead 131 has a substantially flat profile so as to allow an easy wire bonding thereon. Also, as shown in FIG. 1(b), because the third and fourth faces 131Ac and 131Ad have a concave shape which is depressed toward the inside of the associated inner lead, a high strength can be obtained even though the second face (wire bonding surface) 131Ab is narrowed.

In the present embodiment, since twisting does not

occur in the inner leads 131 irrespective of whether the inner leads 131 is long or not. The inner leads having the contour, as shown in FIG. 9(a), in which the tips of the inner leads 131 are separated one from another, are prepared by the etching process, and the inner leads are resin-encapsulated after mounting the semiconductor chip thereon as will be described later. However, where the inner leads 131 are long in their length and have a tendency for the generation of twisting therein, it is impossible to fabricate the lead frame by etching to have the contour as shown in FIG. 9(a). Therefore, after etching the lead frame in a state where the tips of the inner leads are fixed to the connecting portion 131B as shown in FIG. 9(c)(1), the inner leads 131 are fixed with the reinforcing tape 160 as shown in FIG. 9(c)(2). Then, the connecting portions 131B which are not necessary in the fabrication of the resin-encapsulated semiconductor device are removed by a press as shown in FIG. 9(c)(3), and a semiconductor device is then mounted on the lead frame.

Hereinafter, a method for the fabrication of the resin-encapsulated semiconductor device will now be described with reference to FIG. 8. First, the lead frame 130A, as shown in FIG. 9(a), which is shaped by the etching process as will be described later, is prepared such that the second surfaces 131Ab of the inner leads 131 are

directed upward (FIG. 8(a)).

Then, the semiconductor chip 110 is mounted onto the die pad 135 such that the surfaces of the semiconductor chip 110 on which the electrodes 111 are arranged, are directed upward (FIG. 8(b)).

Next, after the semiconductor chip 110 is fastened onto the die pad 135, the electrodes 111 of the semiconductor chip 110 and the second surfaces 131ab of the inner leads 131 are bonded with each other using wires 110 (FIG. 8(c)).

Subsequently, encapsulation is carried out with the conventional resin encapsulate 140. Thereafter, unnecessary portions of the lead frame 130 which are protruded from the resin encapsulate 140 are cut by a press to form terminal columns 133 and also the side surfaces 133B of the terminal columns 133 (FIG. 8(d)).

Then, the dam bars 136, the frame portions 137, etc. of the lead frame 130A as shown in FIG. 9 are removed. Next, the terminal portions 133A each made of the semi-spherical solder are arranged on the outer surface of each terminal column 133 to fabricate a resin-encapsulated semiconductor device (FIG. 8(e)).

Thereafter, the protective frame 180 is arranged by means of adhesive around an entire outer surface of the resultant structure in such a manner that the side surfaces

of the terminal columns 133 are covered thereby FIG. 6(f)). At this time, the protective frame 180 functions to reinforce the semiconductor device. In other words, the protective frame 180 serves to prevent moisture from
5 leaking into a gap between the resin encapsulate and the terminal columns due to the fact that the side surfaces of the terminal columns are exposed to the outside, whereby a crack is not formed in the semiconductor device and the breakage of the semiconductor device is avoided. However,
10 persons skilled in the art will readily appreciate that it is not necessarily required to provide the protective frame 180. Also, when such an encapsulating process by the resin is carried out using a desired mold, the encapsulating process is implemented in a state wherein the outer side
15 surfaces of the terminal columns of the lead frame are somewhat protruded out of the resin encapsulate.

A method for etching the lead frame of the first embodiment will now be described in conjunction with the attached drawings. FIG. 11 is of cross-sectional views
20 respectively illustrating sequential steps of the etching process for the lead frame of the first embodiment. In particular, the cross-sectional views of FIG. 1 correspond to a cross section taken along the line D1-D2 of FIG. 9(a). In FIG. 11, the reference numeral 1110 denotes a lead frame
25 blank, 1120A and 1120B resist patterns, 1130 first opening,

1140 second openings, 1150 first concave portions, 1160 second concave portions, 1170 flat surfaces, and 1180 an etch-resistant layer. First, a water-soluble casein resist using potassium dichromate as a sensitive agent is coated
5 over both surfaces of the lead frame blank 1110 made of a 42% nickel-iron alloy and having a thickness of about 0.15 mm. Using desired pattern plates, the resist films are patterned to form resist patterns 1120A and 1120B having first opening 1130 and second openings 1140, respectively
10 (FIG. 11(a)).

The first opening 1130 is adapted to etch the lead frame blank 1110 to have a flat etched bottom surface to a thickness smaller than that of the lead frame blank 1110 in a subsequent process. The second openings 1140 are adapted
15 to form desired shapes of tips of inner leads. Although the first opening 1130 includes at least an area forming the tips of the inner leads 1110, a topology generated by partially thinned portion by etching in a subsequent process can cause hindrance in a taping process or a
20 clamping process for fixing the lead frame. Thus, an area to be etched needs to be large without being limited to fine portions of the tips of the inner leads. Thereafter, both surfaces of the lead frame blank 1110 formed with the resist patterns are etched using a 48 Be ferric chloride
25 solution of a temperature of 57°C at a spray pressure of

2.5 kg/cm². The etching process is terminated at the point of time when first recesses 1150 etched to have a flat etched bottom surface have a depth h corresponding to 2/3 of the thickness of the lead frame blank (FIG. 11a).

5 Although both surfaces of the lead frame blank 1110 are simultaneously etched in the primary etching process, it is not necessary to simultaneously etch both surfaces of the lead frame blank 1110. The reason why both surfaces of the lead frame blank 1110 are simultaneously etched, as in
10 this embodiment, is to reduce the etching time taken in a secondary etching process as will be described later. The total time taken for the primary and secondary etching processes is less than that taken in the case of etching of only one surface of the lead frame blank on which the resist pattern 1120B is formed. Subsequently, the surface
15 provided with the first recesses 1150 respectively etched at the first opening 1130 is entirely coated with an etch-resistant hot-melt wax (acidic wax type MR-WB6, The Inctec Inc.) by a die coater to form an etch-resistant layer 1180 so as to fill up the first recesses 1150 and to
20 cover the resist pattern 1120A (FIG. 11(c)).

It is not necessary to coat the etch-resistant layer 1180 over the entire portion of the surface provided with the resist pattern 1120A. However, it is preferred that
25 the etch-resistant layer 1180 be coated over the entire

portion of the surface formed with the first recess
and first opening 1130, as shown in FIG. 11(c), be-
is difficult to coat the etch-resistant layer 1180 o
the surface portion including the first recesses.
5 Although the etch-resistant layer 1180 wax employed i
embodiment is an alkali-soluble wax, any suitabl
resistant to the etching action of the etchant solutio
remaining somewhat soft during etching may be used.
for forming the etch-resistant layer 1180 is not limit
10 the above-mentioned wax, but may be a wax of a UV-se
type. Since each first recess 1130 etched by the pr
etching process at the surface formed with the pa
adapted to form a desired shape of the inner lead t
filled up with the etch-resistant layer 1180, it is
15 further etched in the following secondary etching pro
The etch-resistant layer 1180 also enhances the mechan
strength of the lead frame blank for the second etc
process, thereby enabling the second etching process to
conducted while keeping a high accuracy. It is
20 possible to enable a second etchant solution to be spr
at an increased spraying pressure, for example, 2.5 kg
or above, in the secondary etching process. The increa
spraying pressure promotes the progress of etching in
direction of the thickness of the lead frame blank in
25 secondary etching process. Then, the lead frame blank

subjected to a secondary etching process. In this secondary etching process, the lead frame blank 1110 is etched at its surface formed with first recesses 1130 having a flat etched bottom surface, to completely perforate the second recesses 1160, thereby forming the tips of inner leads 131A (FIG. 11B)).

The bottom surface 1170 of each recess formed by the primary etching process is flat. However, both side surfaces of each recess positioned at opposite sides of the bottom surface 1170 have a concave shape depressed toward the inside of the inner lead. Then, the lead frame blank is cleaned. After completion of the cleaning process, the etch-resistant layer 1180, and resist films (resist patterns 1120A and 1120B) are sequentially removed. Thus, a lead frame 130A having a structure of FIG. 9(a) is obtained in which tips of the inner leads 131A are arranged at a fine pitch. The removal of the etch-resistant layer 1180 and resist films (resist patterns 1120A and 1120B) is achieved using a sodium hydroxide solution serving to dissolve them.

The processes for manufacturing the lead frame as shown in FIG. 11, is to form by means of etching the lead frame having the tips of the inner leads used in this embodiment of the present invention, which have a thickness less than that of the lead frame. Especially, the first

surfaces 131Aa of the tips of the inner leads as shown in
FIG. 1, are flushed with one surfaces of remaining portions
of the inner leads having the same thickness with the lead
frame while being opposed to the second surfaces 131Ab, and
5 the third and fourth surfaces are formed to have a concave
shape which is depressed toward the inside of the inner
leads. Where a semiconductor chip is mounted on the second
surfaces 131Ab of the inner leads by means of bumps for an
electrical connection therebetween, as in a semiconductor
10 device according to a third embodiment as will be described
hereinafter, an increased tolerance for the connection by
bumps is obtained when the second surface 131Ab has a
concave shape depressed toward the inside of the inner
lead. To this end, an etching method shown in FIG. 12 is
15 adopted in this case. The etching method shown in FIG. 12
is the same as that of FIG. 11 in association with its
primary etching process. After completion of the primary
etching process, the etching method is conducted in a
manner different from that of the etching method of FIG. 11
20 in that the second etching process is conducted at the side
of the first recesses 1150 after filling up the second
recesses 1160 by the etch-resist layer 1180, thereby
completely perforating the second recesses 1160. At this
time, by implementing the primary etching process, etching
25 at the side of the second openings 1140 is performed in a

sufficient manner. The cross section of each inner lead, including its tip, formed in accordance with the etching method of FIG. 12, has a concave shape depressed toward the inside of the inner lead at the second surface 131Ab, as shown in FIG. 6(b).

The etching method in which the etching process is conducted at two separate steps, respectively, as in that of FIGs. 11 and 12, is generally called a "two-step etching method". This etching method is advantageous in that a desired fineness can be obtained. The etching method used to fabricate the lead frame 130A of the first embodiment shown in FIG. 9 involves the two-step etching method and the method for forming a desired shape of each lead frame portion while reducing the thickness of each pattern formed. In particular, the etching method makes it possible to achieve a desired fineness. In accordance with the method illustrated in FIGs. 11 and 12, the fineness of the tip of each inner lead 131A formed by this method is dependent on the shape of the second recesses 1160 and the thickness t of the inner lead tip which is finally obtained. For example, where the blank has a thickness t reduced to 50 μ m, the inner leads can have a fineness corresponding to a lead width W_1 of 100 μ m and a tip pitch p of 0.15 mm, as shown in FIG. 11(e). In the case of using a small blank thickness t of about 30 μ m and a lead

width W_1 of 70 μm , it is possible to form inner leads having a fineness corresponding to an inner lead pitch p of 0.12 mm. Of course, it may be possible to form inner leads having a further reduced tip pitch by adjusting the blank thickness t and the lead width W_1 . That is to say, an inner lead tip pitch p up to 0.08 mm, a blank thickness up to 25 μm , and a lead width W_1 up to 40 μm can be obtained.

In the case where twisting of the inner leads does not occur in the fabricating process, as in the case where the inner leads are short in their length, a lead frame illustrated in FIG. 9(a) can be directly obtained. However, where the inner leads are long in length as compared to those of the first embodiment, the inner leads have tendency for the generation of twisting. Thus, in this case, the lead frame is obtained by etching in a state where the tips of the inner leads are bound to each other by a connecting member 131B as shown in FIG. 9(c)(1). Then, the connecting member 131B which is not necessary for the fabrication of a semiconductor package is cut off by means of a press to obtain a lead frame shaped as shown in FIG. 9(a).

Moreover, as described above, where unnecessary portions in a structure shown in FIG. 9(c)(1) are cut to obtain the lead frame having the contour shown in FIG.

9(a), a reinforcing tape 160 (a polyimide tape is generally used, as shown in FIG. 9(b)(A)). While the connecting member 131B is cut off by means of a press to obtain the contour shown in FIG. 9(c)(D), a semiconductor device is mounted on the lead frame still having the reinforcing tape attached thereon. Also, the mounted semiconductor device is encapsulated with a resin in a condition where the lead frame still has the tape. The line E11-E12 illustrates a cut portion.

The tip of the inner lead 131 of the lead frame used in the semiconductor device of this first embodiment has a cross-sectional shape as shown in FIG. 13(1)(a). The tip 131A has an etched flat surface (second surface) 131Ab which is substantially flat and therefore has a width $W1$ slightly greater than the width $W2$ of an opposite surface. The widths $W1$ and $W2$ (about 1000 μm) are more than the width W at the central portion of the tips when viewed in the direction of the inner lead thickness. Thus, the tip of the inner lead has a cross-sectional shape having opposite wide surfaces. To this end, although either of the opposite surfaces of the tip 131A can be easily electrically connected to a semiconductor device (not shown) by a wire 120A or 120B, this embodiment illustrates the use of the etched flat surface for wire-bonding as shown in FIG. 13(D)(a). In FIG. 13, a reference numeral

131Ab depicts an etched flat surface, 131Aa a surface of a lead frame blank, and 121A and 121B, respectively, a plated portion. In the case of FIG. 13(D)(a), there has particularly excellent in wire-bonding property, because
5 the etched flat surface does not have roughness. FIG. 13(A) shows that the tip 1331B of the inner lead of the lead frame fabricated according to the process illustrated in FIG. 14 is wire-bonded to a semiconductor device. In this case, however, both the opposite surfaces of the tip
10 1331B of the inner lead are flat, but have a width smaller than that in a direction of the inner lead thickness. In addition to this, as both the opposite surfaces of the tip 1331B is formed of surfaces of the lead frame blank, these surfaces have an inferior wire-bonding property as compared
15 to that of the etched flat surface of this first embodiment. FIG. 13(=) shows that the inner lead tip 1331C or 1331D, obtained by thinning in its thickness by a means of a press (coining) and then by etching, is wire-bonded to a semiconductor device (not shown). In this
20 case, however, a pressed surface of the inner lead tip is not flat as shown FIG. 13(=). Thus, the wire-bonding on either of the opposite surfaces as shown in FIG. 13(=)(a) or FIG. 13(=)(b) often results in an insufficient wire-bonding stability and a problematic quality. The drawing
25 reference numeral 1331Ab represents a coining surface.

A modified example of the resin-encapsulated semiconductor device in accordance with the first embodiment of the present invention will be described hereinafter. FIGs. 3(a) through 3(e) are cross-sectional views of the modified example of the resin-encapsulated semiconductor device in accordance with the first embodiment of the present invention. The semiconductor device of the modified example as shown in FIG. 3(a), is different from that of the first embodiment in that a position of the die pad 135 is changed, that is, the die pad 135 is exposed to the outside. By the fact that the die pad 135 is exposed to the outside, the heat dissipation property is improved as compared to the first embodiment. Also, in the semiconductor device of the modified example as shown in FIG. 3(b), because the die pad 135 is exposed to the outside, the heat dissipation property is improved as compared to the first embodiment. Unlike the first embodiment or the modified example as shown in FIG. 3(a), in the present modified example as shown in FIG. 3(b), because a direction of the semiconductor device 110 is changed, the first surfaces of the lead frame are established as the wire bonding surfaces. The modified examples as shown in FIGs. 3(c), 3(d) and 3(e), illustrate semiconductor devices which are obtained by modifying the semiconductor devices of the first embodiment, the modified

example as shown in FIG. 3(a) and the modified example as shown in FIG. 3(b), wherein the semi-spherical solders are not used, and instead, the top surfaces of the terminal columns are directly used as the terminal portions, whereby
5 an entire manufacturing procedure can be simplified.

Next, a resin-encapsulated semiconductor device in accordance with a second embodiment of the present invention will be described. FIG. 4(a) is a cross-sectional view of the resin-encapsulated semiconductor
10 device in accordance with the second embodiment of the present invention, FIG. 4(b) is a cross-sectional view illustrating inner leads, taken along the line A3-A4 of FIG. 4(a), and FIG. 4(c) is a cross-sectional view illustrating a terminal column, taken along the line B3-B4
15 of FIG. 4(a). Because an outer appearance of the semiconductor device of the second embodiment is substantially the same as that of the first embodiment, it is not illustrated in the drawings. In FIG. 3, the drawing reference numeral 200 represents a semiconductor device,
20 210 a semiconductor chip, 211 electrodes (pads), 220 wires, 230 a lead frame, 231 inner leads, 231Ab a second surface, 231Ac a third surface, 231Ad a fourth surface, 233 terminal columns, 233A terminal portions, 233B side surfaces, 233S top surfaces, 240 a resin encapsulate, and 270 a
25 reinforcing fastener tape. In the semiconductor device of

this second embodiment, the lead frame 230 does not have a die pad, the semiconductor chip 210 is fastened to the inner leads 231 by the reinforcing fastener tape 270, and the semiconductor chip 210 is electrically connected at its electrodes (pads) 211 to the second surfaces 231Ab of the inner leads 231 by wires 220. Also, in the case of this second embodiment, similarly to the first embodiment, the electrical connection between the resin-encapsulated semiconductor device 200 of this embodiment and an external circuit is achieved by mounting the resin-encapsulated semiconductor device 200 via the terminal portions 233A each being made of a semi-spherical solder, on a printed circuit substrate, with the terminal portions 233A located on the top surfaces 233S of the terminal columns 233, respectively.

In addition, the semiconductor device of this second embodiment does not have a die pad as shown in FIGs. 10(a) and 10(b). The manufacturing method of the semiconductor device of this embodiment using the lead frame 230A which is shaped by the etching process is substantially the same as that of the first embodiment except that, while in the case of the first embodiment, the wire bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip is fastened to the inner leads, in the case of the second embodiment, the wire

bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip 210 is fastened together with the inner leads 231 by the reinforcing fastener tape 270. Also, the cutting process for the unnecessary portions and the terminal portion forming process after resin encapsulating process are implemented in the same way as the first embodiment. The lead frame 230 as shown in FIG. 10(a) is obtained in the same manner by which the lead frame 130A as shown in FIG. 9(a) is obtained. In other words, by cutting the resultant structure obtained after etching the structure as shown in FIG. 10(c)(1), the contour as shown in FIG. 10(a) is obtained. At this time, the conventional reinforcing fastener tape 260 (the polyimide tape) as shown in FIG. 10(c)(2), which performs a reinforcing function is used.

FIG. 5(a) through 5(c) are cross-sectional views illustrating modified examples of the semiconductor device of the second embodiment. The semiconductor device as shown in FIG. 5(a) is different from the semiconductor device of the second embodiment, in that the surface of the semiconductor chip thereof which has the electrodes is directed downward. The modified examples as shown in FIGS. 5(b) and 5(c), illustrate semiconductor devices which are obtained by modifying the semiconductor devices of the second embodiment and the modified example as shown in FIG.

5(a), wherein the semi-spherical solders are not used, and instead, the top surfaces of the terminal columns are directly used as the terminal portions. In these examples, because a protective frame is not used and the side surfaces 333B of the terminal columns 333 are exposed to the outside, a checking operation by a test, etc. can be easily performed.

Hereinafter, a resin-encapsulated semiconductor device in accordance with a third embodiment of the present invention will be described. FIG. 6(a) is a cross-sectional view of the resin-encapsulated semiconductor device of the third embodiment, FIG. 6(b) is a cross-sectional view illustrating inner leads, taken along the line A5-A6 of FIG. 6(a), and FIG. 6(c) is a cross-sectional view illustrating a terminal column, taken along the line B5-B6 of FIG. 6(b). Because an outer appearance of the semiconductor device of the this third embodiment is substantially the same as that of the first embodiment, it is not illustrated in the drawings. In FIG. 6, the drawing reference numeral 300 represents a semiconductor device, 310 a semiconductor chip, 312 bumps, 330 a lead frame, 331 inner leads, 331Aa a first surface, 331Ab a second surface, 331Ac a third surface, 331Ad a fourth surface, 333 terminal columns, 333A terminal portions, 333B side surfaces, 333S top surfaces, 340 a resin encapsulate, and 350 a

reinforcing fastener tape. In the semiconductor device of this third embodiment, the semiconductor chip 310 is fastened to the second surfaces 331Ab of the inner leads 331 by the bumps 311 thereby to be electrically connected to the second surfaces 331Ab. The lead frame 330 has a contour as shown in FIGs. 10(a) and 10(b), which is formed by the etching process of FIG. 11. As shown in FIG. 13(1)(b), both widths W1A and W2A (about 100 μ m) at top and bottom ends of the inner leads 331 are larger than a width WA at a center portion in a thickness-wise direction. Due to the fact that the second surfaces 331Ab of the inner leads 331 is depressed toward the inside of the inner leads and the first surfaces 331Aa are flat, a desired fineness can be obtained. Also, when the second surfaces 331Ab of the inner leads 331 are electrically connected to the semiconductor chip via bumps, easy connection can be accomplished as shown in FIG. 13(2)(b). Further, in the case of this third embodiment, as in the case of the first and second embodiments, the electrical connection between the resin-encapsulated semiconductor device 300 of this embodiment and an external circuit is achieved by mounting the resin-encapsulated semiconductor device 300 via the terminal portions 333A each being made of a semi-spherical solder, on a printed circuit substrate, with the terminal portions 333A located on the top surfaces of the terminal

columns 333, respectively.

In addition, unlike the semiconductor device of the first embodiment, the semiconductor device of this third embodiment uses a lead frame which is shaped by the etching process as shown in FIG. 12. However, the manufacturing method of the semiconductor device of this embodiment is substantially the same as that of the first embodiment except that, while in the case of the first embodiment, the wire bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip is fastened to the inner leads, in the case of this third embodiment, the wire bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip 310 is fastened to the inner leads 331 via the bumps. Also, the cutting process for the unnecessary portions and the terminal portion forming process after resin encapsulating process are implemented in the same way as the first embodiment.

FIG. 6(d) is a cross-sectional view illustrating a modified example of the semiconductor device in accordance with the third embodiment of the present invention. In the modified example of the semiconductor device as shown in FIG. 6(d), the terminal portions each comprising the semi-spherical solder are not provided, and the top surfaces of the terminal columns are directly used as the terminal

portions. Because the protective frame is not used and the side surfaces 333B of the terminal columns 333 are exposed to the outside, a checking operation by a test, etc. can be easily performed.

5 Hereinafter, a resin-encapsulated semiconductor device in accordance with a fourth embodiment of the present invention will be described. FIG. 7(a) is a cross-sectional view of the resin-encapsulated semiconductor device of the fourth embodiment, FIG. 7(b) is a cross-sectional view illustrating inner leads, taken along the line A7-A8 of FIG. 7(a), and FIG. 7(c) is a cross-sectional view illustrating a terminal column, taken along the line 10 B7-B8 of FIG. 7(b). Because an outer appearance of the semiconductor device of the this fourth embodiment is substantially the same as that of the first embodiment, it is not illustrated in the drawings. In FIG. 7, the drawing reference numeral 400 represents a semiconductor device, 15 410 a semiconductor chip, 411 pads, 430 a lead frame, 431 inner leads, 431Aa a first surface, 431Ab a second surface, 431Ac a third surface, 431Ad a fourth surface, 433 terminal columns, 433A terminal portions, 433B side surfaces, 433S top surfaces, 440 a resin encapsulate, and 470 insulating adhesive. In the semiconductor device of this fourth 20 embodiment, one surface of the semiconductor chip 410 on which the pads 411 are disposed is fastened to the second 25

surfaces 431Ab of the inner leads 431 by the insul-
adhesive 470, and the pads 411 and the first surfaces
of the inner leads 431 are electrically connected with
other by wires 420. The semiconductor device of
5 fourth embodiment uses the same lead frame which is use
the third embodiment, which has the contour as shown
FIG. 10(a) and 10(b). Also, in the case of this fourth
embodiment, as in the case of the first and second
embodiments, the electrical connection between the res-
10 encapsulated semiconductor device 400 of this embodiment
and an external circuit is achieved by mounting the res-
encapsulated semiconductor device 400 via the terminal
portions 433A each being made of a semi-spherical solder
on a printed circuit substrate, with the terminal portio-
15 433A located on the top surfaces of the terminal columns
433, respectively.

FIG. 7(d) is a cross-sectional view illustrating
modified example of the semiconductor device in accordance
with the fourth embodiment of the present invention. In
20 the modified example of the semiconductor device as shown
in FIG. 7(d), the terminal portions each comprising the
semi-spherical solder are not provided, and the top
surfaces of the terminal columns are directly used as the
terminal portions. Because the protective frame is not
25 used and the side surfaces 433B of the terminal columns 433

are exposed to the outside, a checking operation by a test, etc. can be easily performed.

(EFFECTS OF THE INVENTION)

5 The present invention provides a resin-encapsulated semiconductor device employing the above-mentioned lead frame, which is capable of meeting a demand for the increased terminal number. Furthermore, the resin-encapsulated semiconductor device in accordance with this invention does not require a process of cutting or bending the dam bars as in the case of using a lead frame having
10 outer leads as shown in FIG. 13(b). As a result of this, the resin-encapsulated semiconductor device does not have a problem in that the outer leads are bent, or a problem associated with coplanarity. In addition to these
15 advantages, the resin-encapsulated semiconductor device has a shortened interconnection length as compared to the QTP or the BGA, whereby the semiconductor device can be reduced in a parasitic capacity, and shortened in a transfer delay
20 time.

59:343 v:

(11) $47 = 8 \times 5 + 7$

(1) 公明 氏 (1991) : 氏 : 氏

這所表示是二

- 1

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【実施例 1】

2 層エッチング加工によりインターリードの厚さがリードフレーム素材の厚さより厚みになるように加工されたリードフレームを用いた半導体装置であつて、前記リードフレームは、リードフレーム素材より厚みのあるインナーリードと、該インナーリードに一体的に形成したリードフレーム素材と同じ厚さの外部回路とを形成するための凹凸の端子柱とを有し、且つ、端子柱はインナーリードの外周側においてインナーリードに対して厚み方向に直交して設けられており、端子柱の先端部に半導体素子からなる端子部を設け、端子部を防止用樹脂層から露出させ、端子柱の外周側の側面を防止用樹脂層から露出させており、インナーリードは、断面形状が四方角で第 1 面、第 2 面、第 3 面、第 4 面の 4 面を有しており、かつ第 1 面はリードフレーム素材と同じ厚さの他の部分の一方の面と同一直線上にあって第 2 面に向を合っており、第 3 面、第 4 面はインナーリードの内側に向かつて凹んだ形状に形成されていることを特徴とする半導体装置。

【実施例 2】 2 層エッチング加工によりインターリードの厚さがリードフレーム素材の厚さより厚みになるように加工されたリードフレームを用いた半導体装置であつて、前記リードフレームは、リードフレーム素材より厚みのあるインナーリードと、該インナーリードに一体的に形成したリードフレーム素材と同じ厚さの外部回路とを形成するための凹凸の端子柱とを有し、且つ、端子柱はインナーリードの外周側においてインナーリードに対して厚み方向に直交して設けられており、端子柱の先端の一部を防止用樹脂層から露出させて端子部とし、端子柱の外周側の側面を防止用樹脂層から露出させており、インナーリードは、断面形状が四方角で第 1 面、第 2 面、第 3 面、第 4 面の 4 面を有しており、かつ第 1 面はリードフレーム素材と同じ厚さの他の部分の一方の面と同一直線上にあって第 2 面に向を合っており、第 3 面、第 4 面はインナーリードの内側に向かつて凹んだ形状に形成されていることを特徴とする半導体装置。

【実施例 3】 図 1 ないし 2 において、半導体素子はインナーリード間に設けられ、該半導体素子の電極部はワイヤにてインナーリードと電気的に接続されていることを特徴とする半導体装置。

【実施例 4】 図 3 において、リードフレームはダイパッドを有しており、半導体素子はダイパッド上に搭載され、固定されていることを特徴とする半導体装置。

【実施例 5】 図 3 において、リードフレームはダイパッドを有しないもので、半導体素子はインナーリードととらに高強度接着テープにより固定されていることを特徴とする半導体装置。

【実施例 6】 図 1 ないし 2 において、半導体素子は半導体素子の電極部の面をインナーリードの第 2 面

に接触させることにより固定されており、該半導体素子の電極部はワイヤによりインナーリードの第 1 面と電気的に接続されていることを特徴とする半導体装置。

【実施例 7】 図 1 ないし 2 において、半導体素子はパンプによりインナーリードの第 2 面に固定されて電気的にインナーリードと接続していることを特徴とする半導体装置。

【発明の効果】

(0001)

【発明の概要】 本発明は、半導体素子の多ピンに対応して、且つ、アフターリードの低コスト（スルー）やアフターリードの半導体（コブラテリヤ）の特性を有する、リードフレームを用いた半導体装置に係る。

(0002)

【従来の技術】 従来の用いられている半導体装置（プラスチックリードフレームパッケージ）は、一般に図 1 (a) に示されるような構造であり、

半導体素子 1510 を搭載するダイパッド 1511 の両側の面との電気的接続を行うためのアフターリード 1513、アフターリード 1513 に一体となったインナーリード 1512、該インナーリード 1512 の先端部と半導体素子 1520 の電極パッド 1521 とを電気的に接続するためのワイヤ 1530、半導体素子 1520 を防止して外からの応力、熱から守る樹脂 1540 面からなっており、半導体素子 1520 をリードフレームのダイパッド 1511 上に搭載した状態で、樹脂 1540 により封止してパッケージとしたもので、半導体素子 1520 の電極パッド 1521 に対応する位置のインナーリード 1512 を必要とするものである。そして、このような樹脂封止型の半導体装置の構造材料として用いられる（参照）リードフレームは、一般には図 1 (b) に示すような構造のもので、半導体素子 1520 を搭載するためのダイパッド 1511 と、ダイパッド 1511 の周囲に設けられた半導体素子と接続するためのインナーリード 1512、該インナーリード 1512 に接続して外部回路との電気的接続を行うためのアフターリード 1513、樹脂封止する際のダムとなるダムバー 1514、リードフレーム 1510 全体を支持するフレーム（基） 1515 を備えており、通常、銅バー、4 2 合金（42% ニッケル - 58% 金）、銅合金のような導電性に優れた金属材料を用い、プレス加工もしくはエッチング法により形成されている。図 1 (b) (c) は、図 1 (b) (イ) に示すリードフレーム 1510 の F1-F3 に示される断面図である。

(0003) このようなリードフレームを用いた樹脂封止型の半導体装置（プラスチックリードフレームパッケージ）において、端子部は電極部小径の増大と半導体素子の高集積化に伴い、小型化かつ電極部との

180を返ける必要はなく、図1(c)に示すような厚さ180を返けない厚さのままでよい。

(0010) 本発明1の半導体装置100に使用のリードフレーム130は、42Xニッケル-銅合金を主成分としたもので、そして、図9(a)に示すような形状をした、エッチングにより形成加工されたリードフレーム130Aを用いたものであり、端子部133部分や他の部分の厚さより薄部に形成されたインターリード部131をもち、ダムバー136は厚部を防止する部となる。図9(a)に示すような形状をした、エッチングにより形成加工されたリードフレーム130Aを、本発明においては用いたが、インターリード部131と端子部133以外には基本的に不要なものであるから、図9(a)の形状に限定はされない。インターリード部131の厚さ1は40μm、インターリード部131以外の厚さ1は0.15mmでリードフレーム130Aの厚さのままである。インターリード部131以外の厚さは0.15mmに厚さを保ち、0.125mm-0.50mm程度でもよい。また、インターリードピッチは0.12mmと保ちピッチで、半導体装置の多素子化に対応できるものとしている。インターリード部131の第2面131Aは半導体でワイヤボンディングし易い形状となっており、図1(b)に示すように、第3面131A(=第4面131A)はインターリード部へ凹んだ形状をしており、第2面131Aはワイヤボンディング面を狭くしても凹部に近いものとしている。

(0011) 本発明1においては、インターリード131の各々が、インターリード131部に凹みが見えたり、図9(a)に示すような、インターリード部がそれぞれ形成された形状のリードフレームをエッチング加工して作製し、凹みに形成する部分により半導体素子を固定して接続防止している。インターリード131が、インターリード131部に凹みを生じ易い場合には、図9(a)に示す形状にエッチング加工することには出来ないため、図9(c1)-(c3)に示すようにインターリード部を凹み部131Bにて固定した状態でエッチング加工した後、インターリード131部を厚さ160で固定し(図9(c))、(c)においてプレスにて、半導体装置100の凹みに半導体素子110を固定し、この状態で半導体素子を固定して半導体装置を作製する。(図9(c))

(0012) 次に本発明1の半導体装置100の製造方法を図8に基づいて順次に説明する。先ず、図9(a)に示すリードフレーム130Aを、インターリード131部の第2面131Aが凹みで上になるようにして固定した。(図8(a))

次いで半導体素子110の電極部111側の面を図3で示すように、半導体素子をダイバッド135上に固定し、図

8(b)に

半導体素子110をダイバッド135に固定した半導体素子110の電極部111とインターリード部112の第2面とをワイヤ120にてボンディングさせた。(図8(c))

次いで、図8(c)の状態で、40で厚部を防止する部、不要なリードフレーム130の厚部140を除去して、半導体素子をプレスにて固定し、半導体素子を固定するとともに端子部133の凹み133Bを形成した。(図8(c))

図9に示すリードフレーム130Aのダムバー136は、フレーム137を形成した。この時、リードフレームの端子部の凹みの面に半導体素子110からなる端子部133Aを形成して半導体装置を作製した。(図8(c))

次いで、図8(c)の状態で、40で厚部を防止する部、不要なリードフレーム130の厚部140を除去して、半導体素子をプレスにて固定し、半導体素子を固定するとともに端子部133の凹み133Bを形成した。(図8(c))

(0013) 本発明1の半導体装置100に使用のリードフレーム130の製造方法を以下、図10に示すように、図10(a)に示すような、インターリード部がそれぞれ形成された形状のリードフレームをエッチング加工して作製し、凹みに形成する部分により半導体素子を固定して接続防止している。インターリード131が、インターリード131部に凹みを生じ易い場合には、図9(a)に示す形状にエッチング加工することには出来ないため、図9(c1)-(c3)に示すようにインターリード部を凹み部131Bにて固定した状態でエッチング加工した後、インターリード131部を厚さ160で固定し(図9(c))、(c)においてプレスにて、半導体装置100の凹みに半導体素子110を固定し、この状態で半導体素子を固定して半導体装置を作製する。(図9(c))

次に本発明1の半導体装置100の製造方法を図8に基づいて順次に説明する。先ず、図9(a)に示すリードフレーム130Aを、インターリード131部の第2面131Aが凹みで上になるようにして固定した。(図8(a))

次いで半導体素子110の電極部111側の面を図3で示すように、半導体素子をダイバッド135上に固定し、図

8(b)に

半導体素子110をダイバッド135に固定した半導体素子110の電極部111とインターリード部112の第2面とをワイヤ120にてボンディングさせた。(図8(c))

次いで、図8(c)の状態で、40で厚部を防止する部、不要なリードフレーム130の厚部140を除去して、半導体素子をプレスにて固定し、半導体素子を固定するとともに端子部133の凹み133Bを形成した。(図8(c))

で、テーピングの工程や、リードフレームを固定するクランプ工程で、ペタはにばりばり部分的に剥がれた部分との差が所定になる場合があるので、エッチングを行うエリアはインターリード先の追加加工部分だけにせず大めにとらねばならない。従って、温度 57°C 、 1.5×10^{-3} m/s の酸化銅ニッケル溶液を用いて、スプレーで 2.5 kg/cm^2 にて、レジストパターンが形成されたリードフレームを 1110 の面をエッチングし、ペタ (平型) に固定された第一の凹部 1150 の底面がリードフレーム厚の約 $2/3$ 程度に達した時点でエッチングを止めた。(図 11 (b))

上述第 1 回目のエッチングにおいては、リードフレームを 1110 の面から同時にエッチングを行ったが、必ずしも面から同時にエッチングする必要はない。本実施例のように、第 1 回目のエッチングにおいてリードフレームを 1110 の面から同時にエッチングする理由は、面からエッチングすることにより、後述する第 2 回目のエッチング時に使用するため、レジストパターン 920 面からのみの面エッチングの場合と比べ、第 1 回目エッチングと第 2 回目エッチングのトータル時間が短縮される。従って、第一の凹部 1130 側の面を固定された第一の凹部 1150 面にエッチング処理 1180 としての面エッチング性のあるホットメルト型ワックス (ブレンデッドニッケルと銅のワックス、登録商標 MR-WB6) を、ダイコートを用いて、塗布し、ペタ (平型) に固定された第一の凹部 1150 に埋め込んだ。レジストパターン 1120 上にもエッチング処理 1180 に塗布された状態とした。(図 11 (c))

エッチング処理 1180 は、レジストパターン 1120 上全面に塗布する必要はないが、第一の凹部 1150 を含む一面にのみ塗布することにした。図 11 (c) に示すように、第一の凹部 1150 とともに、第一の凹部 1130 全面にエッチング処理 1180 を塗布した。本実施例で使用したエッチング処理 1180 は、アルカリ性銅のワックスであるが、基本的にエッチング液に耐性があり、エッチング時にある程度の腐蝕性のあるものが好ましく、特に、上述ワックスに固定された U.V. 硬化型のものでもよい。このようにエッチング処理 1180 をインターリード先の底面を形成するためのパターンが形成された面側の面を固定された第一の凹部 1150 に塗布することにより、後述するエッチング時に第一の凹部 1150 が固定されて剥がれないようにしているとともに、表面面をエッチング加工に耐える腐蝕性のある状態を維持し、スプレーを 2.5 kg/cm^2 (以上) とすることができ、これによりエッチングが面を方向に進行しやすくなる。この後、第 2 回目のエッチングを行う。ペタ (平型) に固定された第二の凹部 1160 底面からリードフレーム厚 1110 をエッチングし、再度、

インターリード先を 1130 A を形成した。(図 11 (c))

第 1 回目のエッチング加工にて作成された、リードフレーム面に形成したエッチング底面は本質であるが、この面を再び 2 面はインターリード側にへこんだ凹部である。従って、再度、エッチング処理 920 の面をレジスト面 (レジストパターン 1120 A、 1120 B) の面を洗い、インターリード先を 1130 A が形成された図 9 (a) に示すリードフレーム 1130 A を形成し、エッチング処理 1180 とレジスト面 (レジストパターン 1120 A、 1120 B) の面を形成したトリウム系溶液により腐蝕させた。

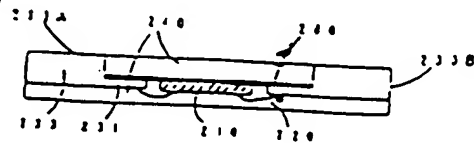
(0014) 上述、図 11 に示すリードフレームの形成方法に、本実施例に用いられる、インターリード先を形成したリードフレームをエッチング加工により形成する方法で、特に、図 11 に示す、インターリード先の第一面 1130 A を形成した後の図 11 (c) の状態に、第二面 1130 B と方向を定めて形成し、且つ、第三面 1130 C、第四面 1130 D をインターリードの内側に向かって凹んだ状態にするエッチング加工方法である。上述する実施例 3 の実施例のようにパンパを用いて本実施例をインターリードの第二面 1130 B に形成し、インターリードと電気的に接続する場合に

は、第二面 1130 B をインターリード側に凹んだ状態に形成した方がパンパ圧力の伝達率が大きくなる。図 12 に示すエッチング加工方法は、第 1 回目のエッチング工程までは、図 11 に示す方法と同じであるが、エッチング処理 1180 を第二の凹部 1160 側に埋め込んだ後、第一の凹部 1150 側から第 2 回目のエッチングを行い、再度凹ませた状態になっている。第 1 回目のエッチングにて、第二凹部 1140 からのエッチングを充分に行っており、図 12 に示すエッチング加工方法によって得られたリードフレームのインターリード先の断面形状は、図 6 (b) に示すように、第二面 1130 B がインターリード側にへこんだ凹部になる。

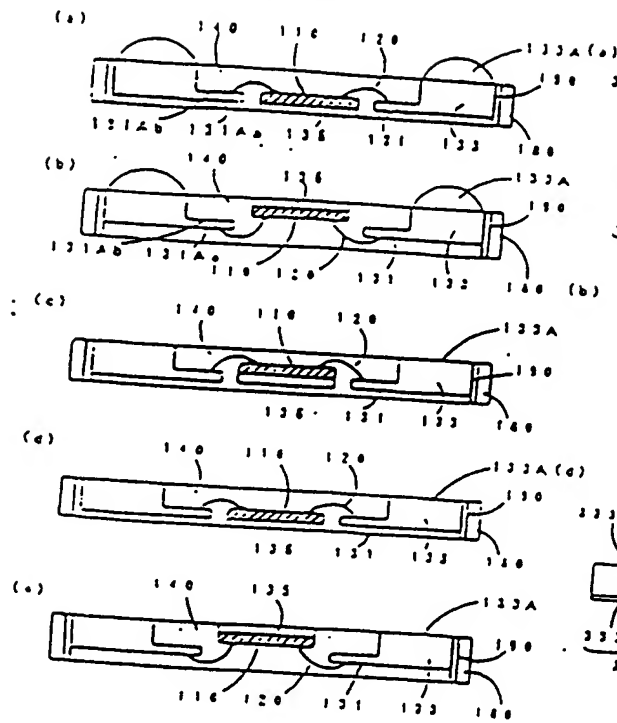
(0015) 図 11、図 12 に示すエッチング加工方法のように、エッチングを 2 段階にわたって行うエッチング加工方法を、一面には 2 段階エッチング加工方法とあり、又は加工に有利な加工方法である。本実施例に用いた図 9 (a) に示す、リードフレーム 1130 A の形成においては、2 段階エッチング加工方法で、パンパを加工することにより部分的にリードフレームを薄くしながら形成する方法とが採用してあり、リードフレームを薄くした部分においては、特に、腐蝕加工が容易なようにしている。図 11、図 12 に示す、上述の方法においては、インターリード先を 1130 A の形成加工は、第二の凹部 1160 の底面と、電気的に用いられるインターリード先の底面とに形成されるもので、例えば、厚さ $150 \mu\text{m}$

190		ードフレイムニ面	
260	1331A6	イニング面	
270	1410	ードフレイムニ面	
280	1420	オートレジスト	
290	1430	ジストパターン	
300	1440	ンターリード	
310	1510	ードフレイム	
320	1511	イパッド	
330	1512	ンターリード	
340	1512A	ンターリード先頭部	
350	1513	ウターリード	
360	1514	ムパー	
370	1515	レーム部 (パッド)	
380	1520	ニ	
390	1521	ニ	
400	1530	ニ	
410	1540	ニ	
420	1540	ニ	
430	1540	ニ	
440	1540	ニ	
450	1540	ニ	
460	1540	ニ	
470	1540	ニ	
480	1540	ニ	
490	1540	ニ	
500	1540	ニ	
510	1540	ニ	
520	1540	ニ	
530	1540	ニ	
540	1540	ニ	
550	1540	ニ	
560	1540	ニ	
570	1540	ニ	
580	1540	ニ	
590	1540	ニ	
600	1540	ニ	
610	1540	ニ	
620	1540	ニ	
630	1540	ニ	
640	1540	ニ	
650	1540	ニ	
660	1540	ニ	
670	1540	ニ	
680	1540	ニ	
690	1540	ニ	
700	1540	ニ	
710	1540	ニ	
720	1540	ニ	
730	1540	ニ	
740	1540	ニ	
750	1540	ニ	
760	1540	ニ	
770	1540	ニ	
780	1540	ニ	
790	1540	ニ	
800	1540	ニ	
810	1540	ニ	
820	1540	ニ	
830	1540	ニ	
840	1540	ニ	
850	1540	ニ	
860	1540	ニ	
870	1540	ニ	
880	1540	ニ	
890	1540	ニ	
900	1540	ニ	
910	1540	ニ	
920	1540	ニ	
930	1540	ニ	
940	1540	ニ	
950	1540	ニ	
960	1540	ニ	
970	1540	ニ	
980	1540	ニ	
990	1540	ニ	
1000	1540	ニ	

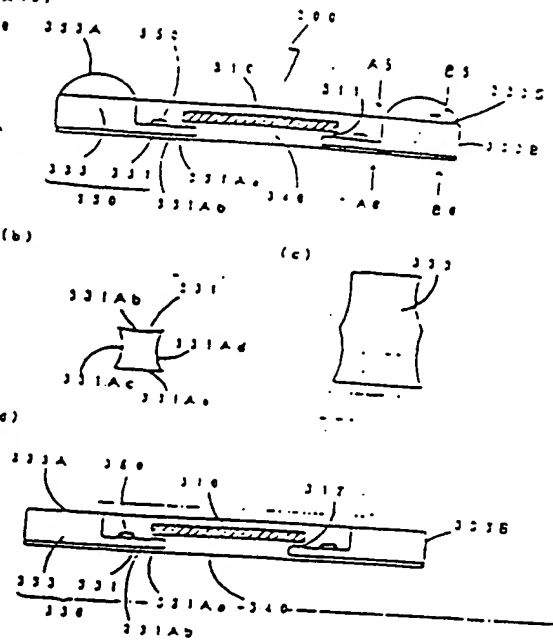
(2)



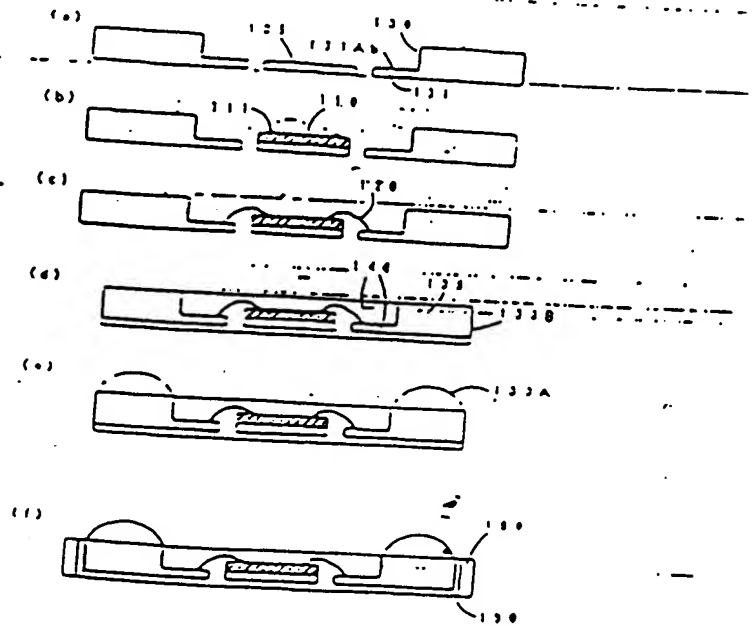
(23)



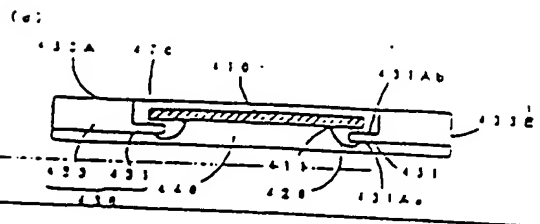
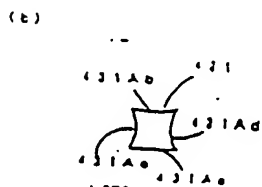
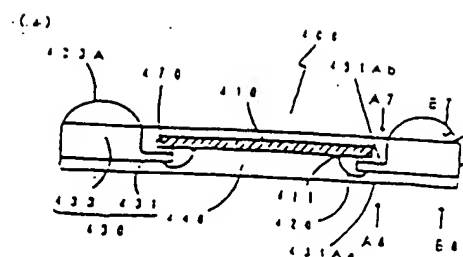
(26)



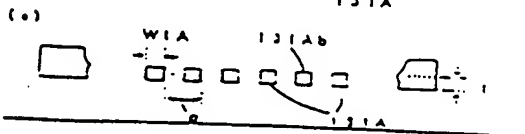
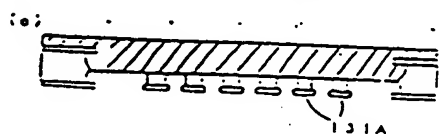
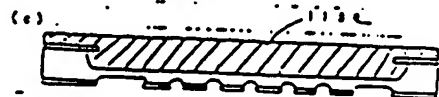
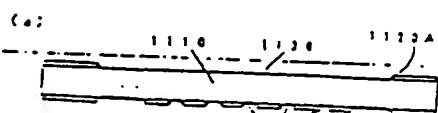
(25)



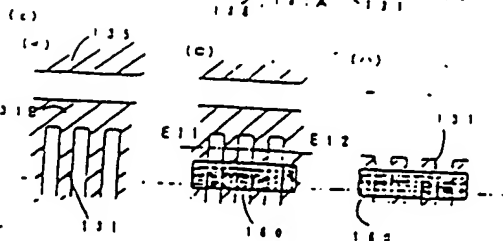
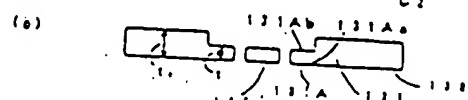
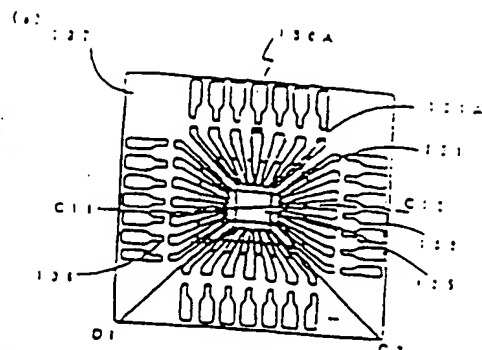
(३१)



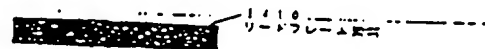
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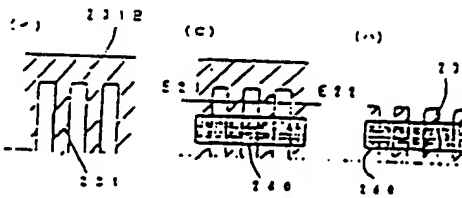
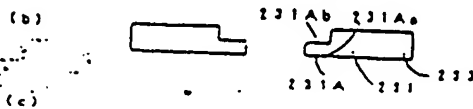
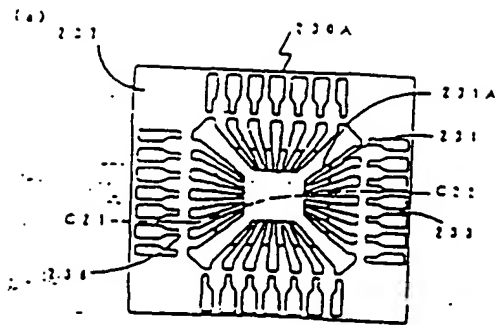
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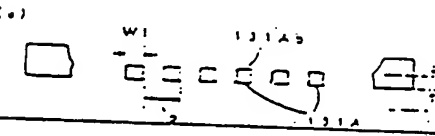
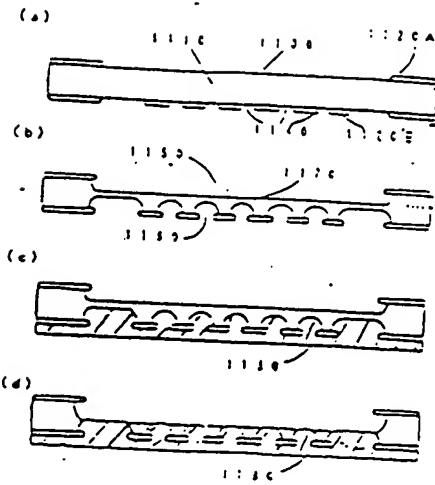
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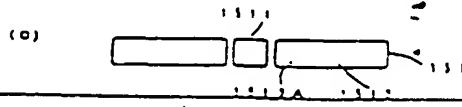
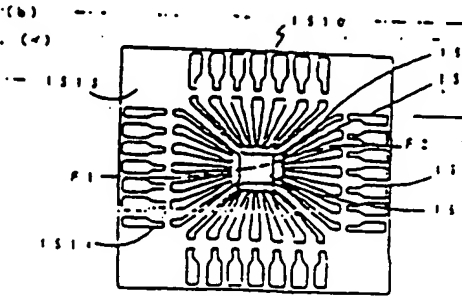
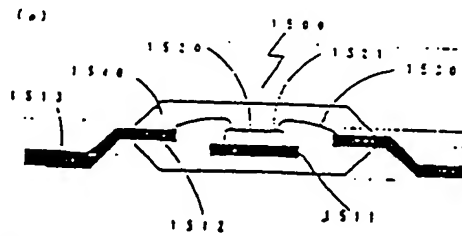
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